



TaiXin AH Module Hardware Design Guide



珠海泰芯半导体有限公司

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Confidential Level	A	TaiXin AH Frequency Setting Instructions	Document Number	
Date	2024-01-09		Document Version	V3.6

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Table of Contents

1.Overview	1
2.Schematic Design	2
2.1.Power Supply	2
2.1.1.System Main Power Supply(VCC0/VCC1/VCC2)	2
2.1.2.SVCC Power Supply	5
2.1.3.1.3V Power Supply (VDD13A/VDD13D)	5
2.1.4.Power-Up Sequence	6
2.2.NorFlash	7
2.3.Reset	8
2.4.RF	8
2.4.1.RF Pi Network	8
2.4.2.Dual Antenna Reference	9
2.5.Interface	9
2.5.1.SDIO	9
2.5.2.Ethernet RMII	11
2.5.3.USB	13
2.5.4.UART	13
2.5.5.SPI	15
2.6.Low Power Consumption	15
2.6.1.STA Low Power Consumption	15
2.6.2.AP Low Power Consumption	17
3.PCB Design	21
3.1.PCB Design Points	21
3.2.Module Placement on the Baseboard	21
3.3.Power Supply	21
3.4.RF	22
3.5.Interfaces	22
3.5.1.USB	22
3.5.2.SDIO	22
3.5.3.RMII	22
3.5.4.UART	23
4.PCB-Level EMI Measurement Method	24
5.Methods for Improving RF Interference with Audio	26



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Confidential Level	A	TaiXin AH Frequency Setting Instructions	Document Number	
Date	2024-01-09		Document Version	V3.6

5.1.Layout Recommendations 26

5.2.Circuit Optimization References 26

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Confidential Level	A	TaiXin AH Frequency Setting Instructions	Document Number	
Date	2024-01-09		Document Version	V3.6

Revision History

Date	Version	Revision Notes	Reviser
2024-01-09	V3.6	Modified the description of the 1.3V supply;	WY
2023-09-07	V3.5	Modified the voltage range for VCC;	WY
2023-06-21	V3.4	Added layout suggestions for audio and RF;	WY
2023-04-03	V3.3	Revised the explanation for sleep wake and AP low power consumption;	WY
2022-12-19	V3.2	Added PCB trace reference for RF; Added suggestions for SDIO clock frequency;	WY
2022-09-22	V3.1	Revised the description of power-up sequence;	WY
2022-08-24	V3.0	Revised the description of low power consumption current;	WY
2022-08-19	V2.9	Revised the explanation for 3.3V ripple;	WY
2022-08-03	V2.8	Added methods to improve RF interference with audio;	YJZ
2022-07-14	V2.7	Modified the explanation for power supply;	WY
2022-05-30	V2.6	Added EMI prevention measures for SDIO;	WY
2022-05-20	V2.5	Adjusted the connection method for SVCC ; Added an explanation for the 1.3V DCDC converter;	WY
2022-02-28	V2.4	Added ferrite bead to VCC1;	WY
2022-02-18	V2.3	Modified the logo;	XYJ
2022-01-10	V2.2	Modified header and footer;	WY
2021-12-16	V2.1	Added an explanation for NorFlash;	WY
2021-09-14	V2.0	Merged with the low power consumption hardware design guide into one document; Added an explanation for AP low power consumption; Included reference for dual antennas;	WY
2021-05-30	V1.7	Added an explanation for SDIO SVCC 1.8V;	WY
2021-05-15	V1.6	Added methods for measuring board-level EMI;	WY
2021-04-19	V1.5	Revised the series resistor value for UART to 1K;	WY
2021-03-10	V1.4	Revised the requirement for the rated current of the power supply;	WY



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Confidential Level	A	TaiXin AH Frequency Setting Instructions	Document Number	
Date	2024-01-09		Document Version	V3.6
2020-12-11	V1.3	Made compatible with the TX-AH-R900X-XX module;		Xue
2020-10-27	V1.2	Modified the pull-up resistor for SDIO;		WY
2020-10-19	V1.1	Adjusted the table of contents;		WY
2020-10-17	V1.0	Initial version		Xue

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1. Overview

The TX-AH module is a highly integrated 802.11AH module operating in the Sub1G frequency band, designed for various applications such as security monitoring, the Internet of Things (IOT), smart homes, etc. The module is equipped with the SOC TXW830x, which is independently researched and developed by Zhuhai TaiXin Semiconductor and has full intellectual property rights. This module supports secondary development and does not require the use of other microcontrollers or processors. It integrates a wealth of communication interfaces to facilitate customer solution development, including RMII, SDIO, USB, SPI, UART, etc. The TX-AH module supports the IEEE 802.11ah protocol and includes a complete Wi-Fi subsystem, integrating Wi-Fi MAC, Wi-Fi RF and baseband, antenna switch, power amplifier, low-noise amplifier, and other components, providing a complete Wi-Fi solution. For more information and ordering details of the TX-AH module, please refer to the "TaiXin 802.11ah TX-AH-Rx00P Series Module Technical Specification".

2. Schematic Design

The TX-AH module integrates a clock crystal oscillator, 802.11ah SOC, antenna switch, power amplifier(PA), surface acoustic wave filter, and other components. The high level of integration simplifies the hardware design of application solutions. To ensure the working performance of the TX-AH module, this document will provide a detailed introduction to the hardware design specifications and precautions when applying the TX-AH module scheme design.

TX-AH Module Application Scheme Hardware Components Introduction:

- Power Supply
- NorFlash
- Reset Circuit
- RF and Antenna
 - PI Network
 - Dual Antenna
- Interfaces
 - SDIO
 - GMAC
 - USB
 - UART
 - SPI
- Low Power Consumption
 - STA Low Power Consumption
 - AP Low Power Consumption

2.1. Power Supply

2.1.1. System Main Power Supply (VCC0/VCC1/VCC2)

The PIN7 (VCC0) of the TX-AH module is the system power input pin of the module, and PIN4/5 (VCC2) and PIN6 (VCC1) are the RF system power input pins of the module. The supply voltage for VCC0/VCC1/VCC2 is 3.1~3.3V, and it is recommended to use 3.3V by default. The rated current of the AH module's power supply is 600mA@3.3V (transmission power @20dBm). When using a DC-DC power supply, to ensure the Rx performance of RF,

the power ripple of 3.3V needs to be less than 30mV in the Rx state. Figure 2-1 shows the power connection diagram of the TX-AH-R900P as an example. Please note that when the TX-AH module is working in TX, the instantaneous power draw will increase, which may cause the power supply to collapse. Therefore, it is recommended to have at least one 10 μ F capacitor on the power line, which can be used in conjunction with 0.1 μ F and 100pF capacitors. In the TX state, it is necessary to ensure that the power supply is not lower than 3.0V. In addition, a ferrite bead can be considered near the PIN6 pin to suppress high-frequency harmonics, that is, a ferrite bead is needed in series on VCC1. As shown in Figure 2-1.

AH_MODULE

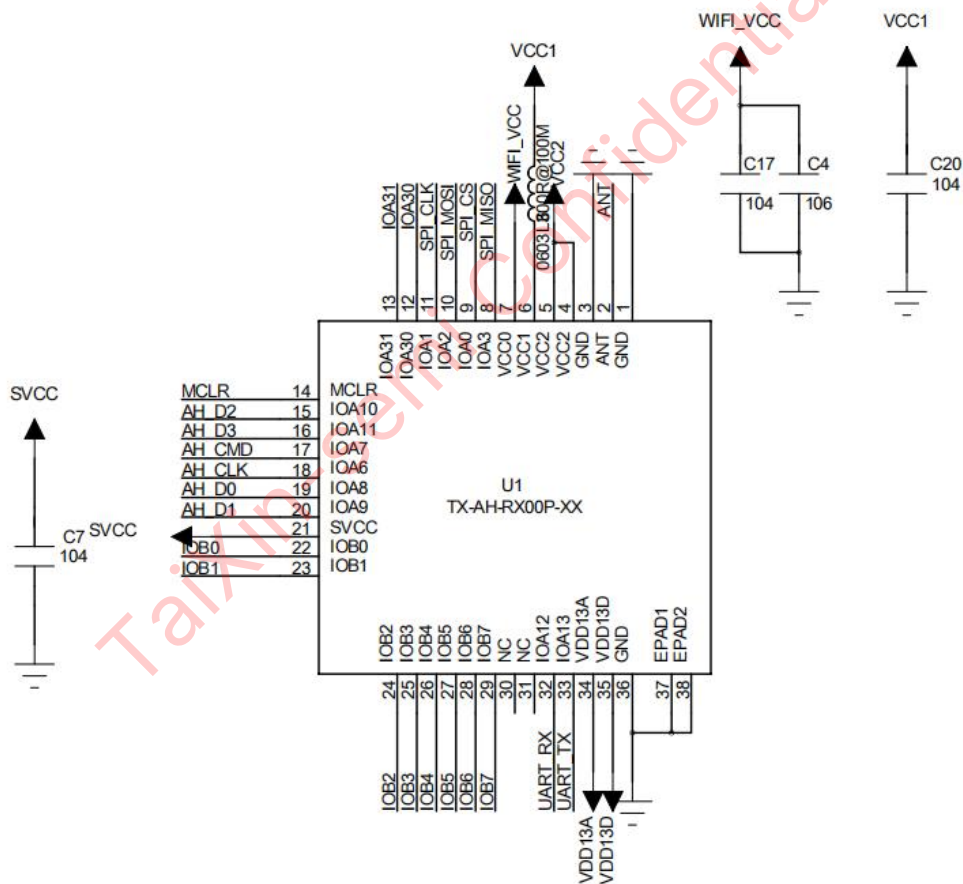


Figure 2-1 TX-AH Module Power Connection

Figure 2-2(a) describes how VCC1 and VCC2 are generated in low power consumption scenarios. In scenarios with high requirements for sleep power consumption (where low power consumption current is less than 250 μ A), VCC1/VCC2 can be disconnected during

sleep. In this case, RF13 should be NC, and IOA30 should be used to control the switching of VCC1/VCC2.

AH LOW PWR MODE CONTROL

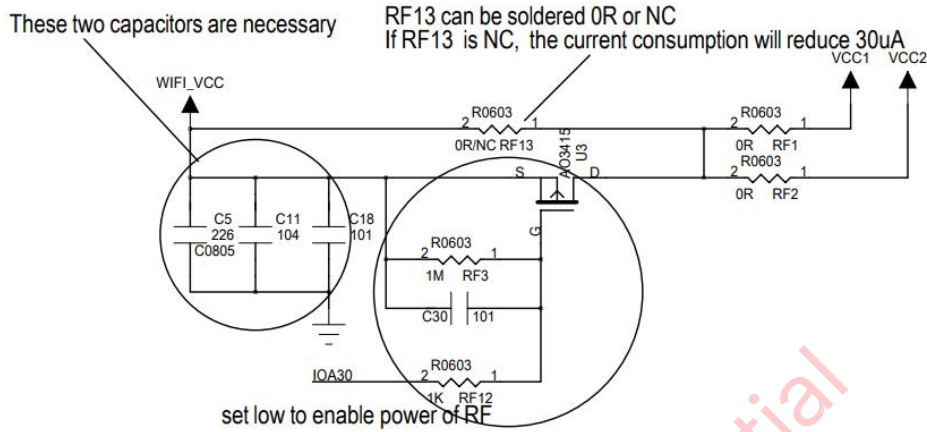


Figure 2-2(a) Power Connection in Low Power Consumption Circuit

If low power consumption scenarios are not a major consideration, VCC0/VCC1/VCC2 can generally be considered connected together. In this case, it is recommended to use a ferrite bead near the PIN6 and PIN7 pins to suppress high-frequency harmonics, that is, **a ferrite bead is needed in series on both VCC1 and VCC0**, as shown in Figure 2-2(b).

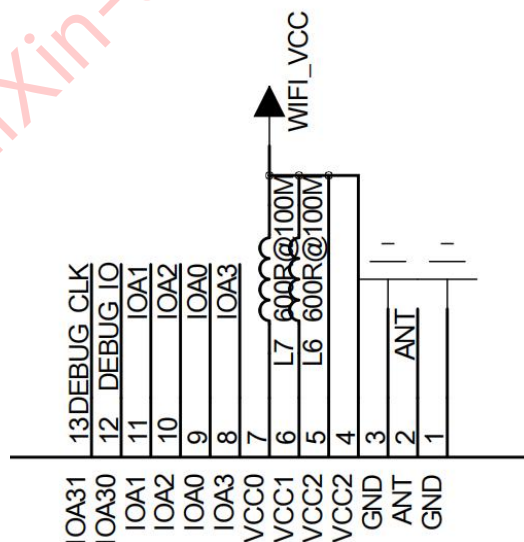


Figure 2-2(b) Power Connection in Non-Low Power Consumption Circuit

2.1.2. SVCC Power Supply

The PIN21 of the TX-AH module is the power input pin for managing the IO voltage IOA6~IOA11, and the SVCC voltage supports an input of 1.8V to 3.3V. The specific input voltage depends on the working voltage level of the host SDIO. If the working voltage level of the host SDIO is 3.3V, then SVCC needs to input 3.3V; if the working voltage level of the host SDIO is 1.8V, SVCC needs to input a fixed 1.8V. If IOA6~IOA11 are multiplexed as other functional pins, in general, it is recommended that SVCC shares the power supply with VCC0, and a 10uF capacitor should be added near the SVCC pin, as shown in Figure 2-3.

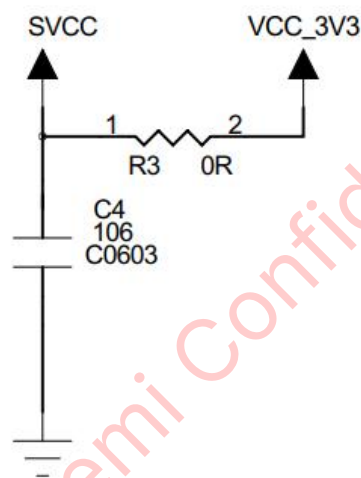


Figure 2-3 SVCC Connection Diagram

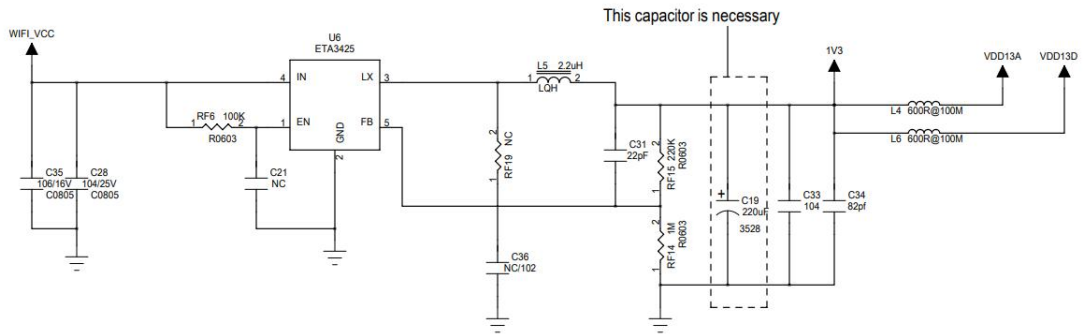
2.1.3. 1.3V Power Supply (VDD13A/VDD13D)

PIN34 and PIN35 are the 1.3V analog and digital power input pins of the AH module: VDD13A and VDD13D, with a recommended voltage range of 1.3~1.35V.

For a low power scheme, an external 1.3V DCDC that supports low power operation is required to reduce overall power consumption. The selection of this DCDC should consider three main parameters: First, the quiescent current of the DCDC should be as low as possible (<20uA) to ensure that the sleep power consumption does not increase significantly; another is to ensure that the DCDC can be in full PWM mode at about 40mA@1.3V, and should not enter PFM or PSM states, as this would degrade Tx/Rx performance in normal mode.

It is recommended to reserve ferrite beads in series for VDD13A and VDD13D to suppress

power ripples. The ripple should be kept within 30mV.



If use this dc/dc, no need to cut-off power due to very low leakage

VDD13(1.3V) current at least 200mA. ripple<30mV

Figure 2-4 1.3V Power Supply Connection Diagram

For non-low power consumption designs, the 1.3V input can be left unconnected, and PIN34/35 can be left floating.

Both STA low power consumption and AP low power consumption require the circuit shown in Figure 2-4.

2.1.4. Power-Up Sequence

If an external 1.3V supplies power to the module, please note that 1.3V should be powered after 3.3V, that is, power up the 1.3V after the 3.3V has been powered.

The AH module needs to pay attention to the situation where the host controller and the TX-AH module are connected via a communication interface. Be sure to confirm the power-on voltage level of the communication interface on the host side.

If the interface power-on voltage level is high while the TX-AH module is not yet powered, the communication interface may leak power to the TX-AH module, causing abnormal startup of the TX-AH module. Please avoid this situation, ensure that the TX-AH module and the host controller are powered up simultaneously.

2.2. NorFlash

The module does not have a built-in SPI NorFlash.

In both the bridge solution and STA low-power solution, an external NorFlash is required. The capacity of the SPI NorFlash should be at least 8Mbit.

For the bridge solution, which is a single module solution, the module must boot from an external NorFlash.

For the STA low-power solution, an external NorFlash is needed to achieve quick wake-up. Without it, downloading firmware via the interface during wake-up would be slow.

Other solutions might consider not using an external NorFlash, instead downloading firmware to the module via the interface. If this method is too slow, using an external NorFlash remains an option.

The reference circuit for the external NorFlash is shown in Figure 2-5. Before selecting a SPI FLASH, please consult the manufacturer to ensure the FLASH model is supported.

SPI BOOT

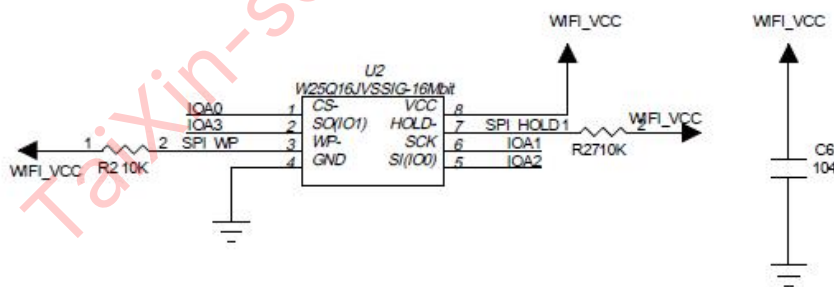


Figure 2-5 NorFlash Circuit

2.3. Reset

The TX-AH module's PIN14 (MCLR) serves as the reset pin. It has an internal weak pull-up, and the reset is active low. To prevent external interference from causing a restart, it is recommended to keep the MCLR trace as short as possible and add an RC circuit at the MCLR pin. (In the STA low-power circuit, MCLR can also be used to wake up the AH module, so pay

attention to the capacitor value).

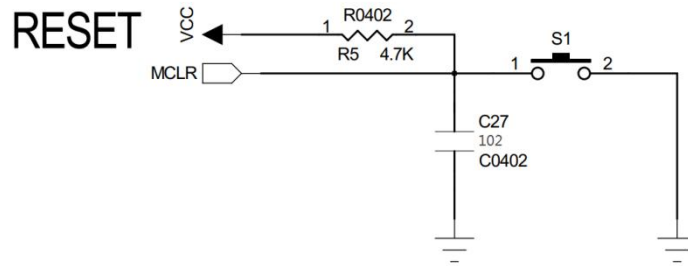
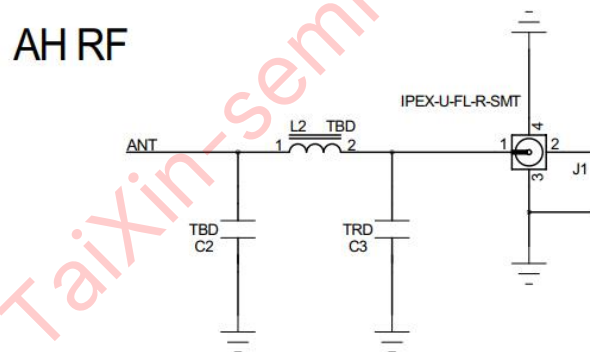


Figure 2-6 Reset Circuit

2.4. RF

2.4.1. RF Pi Network

PIN2 of the TX-AH module is the RF pin. A π -type matching circuit should be reserved in the design, preferably using a CLC structure. The RF circuit of the TX-AH module is shown in Figure 2-7. By default, C2/C3 are NC, and L2 is soldered with 0R.



Pls reserve a "PI" circuit for antenna matching
The RF trace need keep 50ohm impedance.

Figure 2-7 RF Pi Circuit

Note: The parameters of the matching network components need to be determined based on testing with the actual antenna and PCB trace.

2.4.2. Dual Antenna Reference

The AH module supports real-time switching to the antenna with a better signal by detecting the antenna signal. This antenna switching feature is of practical value for some mobile devices or directionally changing devices. The antenna is switched by controlling the external antenna selection switch via IOA31, as shown in Figure 2-8.

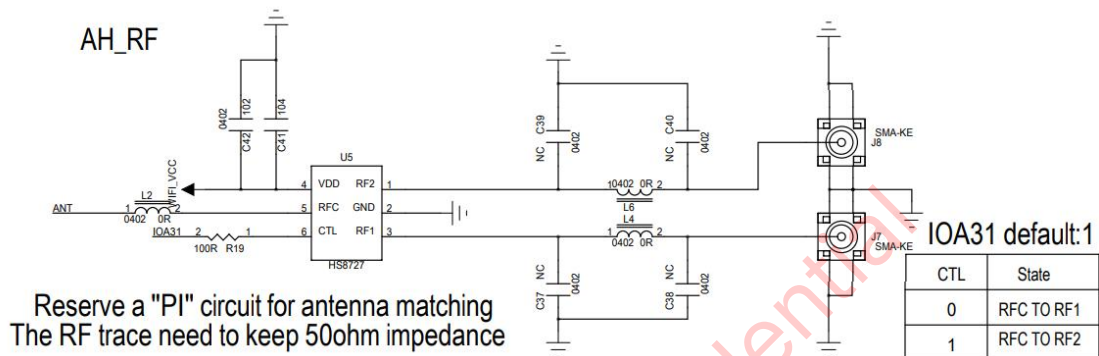


Figure 2-8 Dual Antenna Control Circuit

2.5. Interface

2.5.1. SDIO

When the TX-AH module needs to communicate with the host controller via SDIO, it is recommended to refer to the pin definitions in the "TX-AH Module Specifications" for schematic design. To ensure proper SDIO communication and drive capability, CMD/DATA0~3 should have a 10K pull-up resistor (CLK does not need a pull-up). Additionally, a 22R series resistor should be placed close to the host controller end on the CLK/CMD/DATA0~3 signal lines to suppress high-frequency EMI. An RC filter circuit should be reserved for CLK and placed close to the host controller.

EMI from the SDIO CLK can affect RF performance, so it is recommended to set an appropriate CLK frequency to avoid harmonics in the RF operating bands. For example, setting the frequency to 30MHz/39MHz/45MHz/50MHz will prevent harmonics from falling within the 902M~928M and 863~868M bands. If the CLK frequency cannot be adjusted and its harmonics fall within the RF operating bands, reduce the drive strength to lower EMI.

Pay attention to the input level of SVCC. It is recommended to connect SVCC to the main

controller's power supply rather than to the module's VCC. If the SDIO 3.0 main controller prefers a 1.8V level, it should be fixed at 1.8V and don't go through the 3.3V to 1.8V conversion process.

IOA12/13 are used as debug print ports.

Refer to Figure 2-9 for the schematic design.

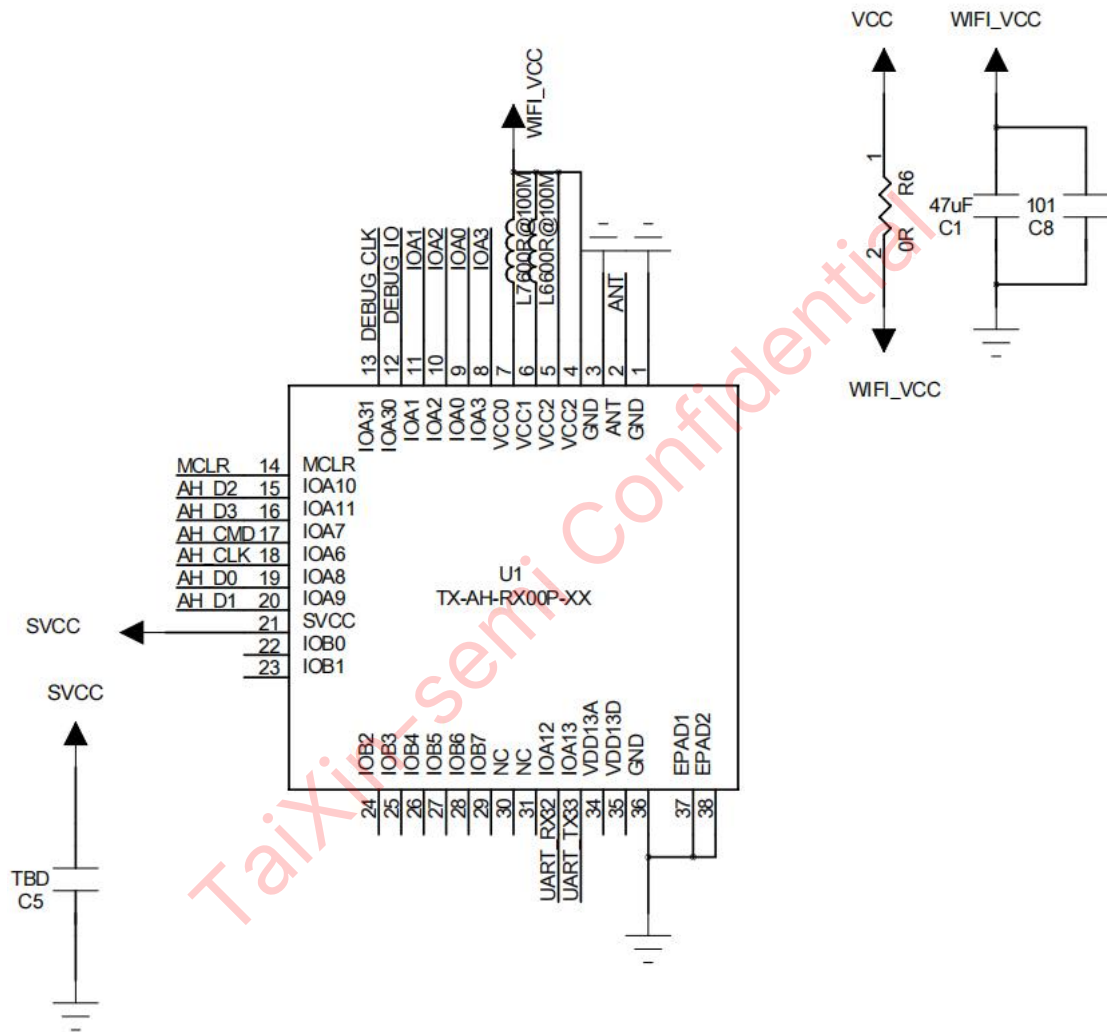


Figure 2-9 (a) SDIO Interface Signal Connection

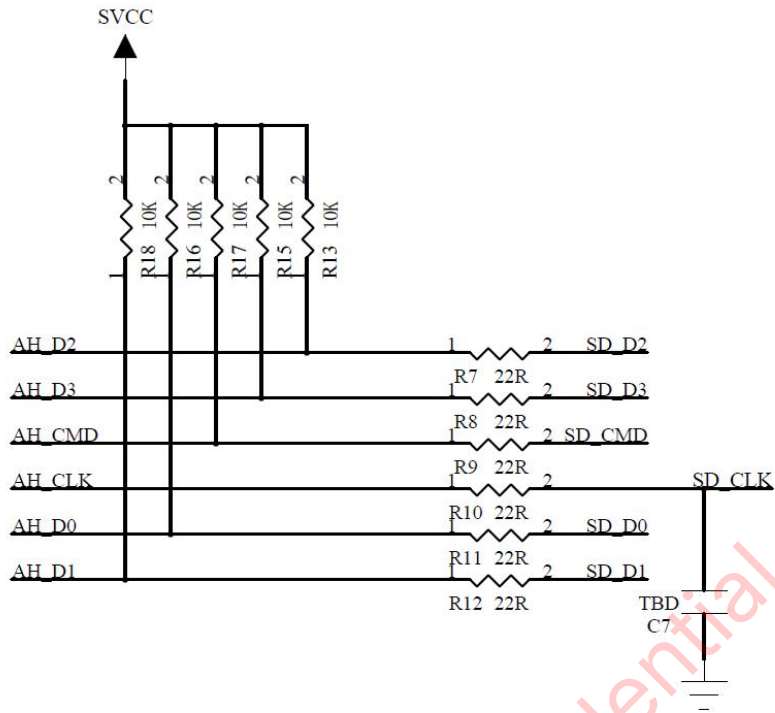


Figure 2-9 (b) SDIO Interface Signal Connection

2.5.2. Ethernet RMII

When the TX-AH module needs to use RMII communication, it is recommended to refer to the pin definitions in the "TX-AH Module Specification" for schematic design. For the TX-AH module trace, refer to Figure 2-10. The input level of SVCC depends on the selected Ethernet PHY, generally 3.3V. It is particularly noted that an RC filter circuit should be reserved for CLK and placed close to the host controller.

IOA12/13 are used as debug print ports.

When selecting an Ethernet PHY, please consult with our company first to ensure the Ethernet PHY is supported. Currently supported PHY models include: IP101GR, RT8201. For other Ethernet PHY models, please contact our FAE.

2.5.3. USB

When the TX-AH module needs to use USB communication, it is recommended to refer to the pin definitions in the "TX-AH Module Specifications". IOA12 and IOA13 are respectively USB DM and DP. It is recommended to reserve series resistors and ground capacitors on the USB lines. IOA10/11 are used as debug print ports. If an exposed interface is needed, a TVS protection diode should be reserved. Refer to Figure 2-11 for the connection details of the TX-AH module.

AH_MODULE

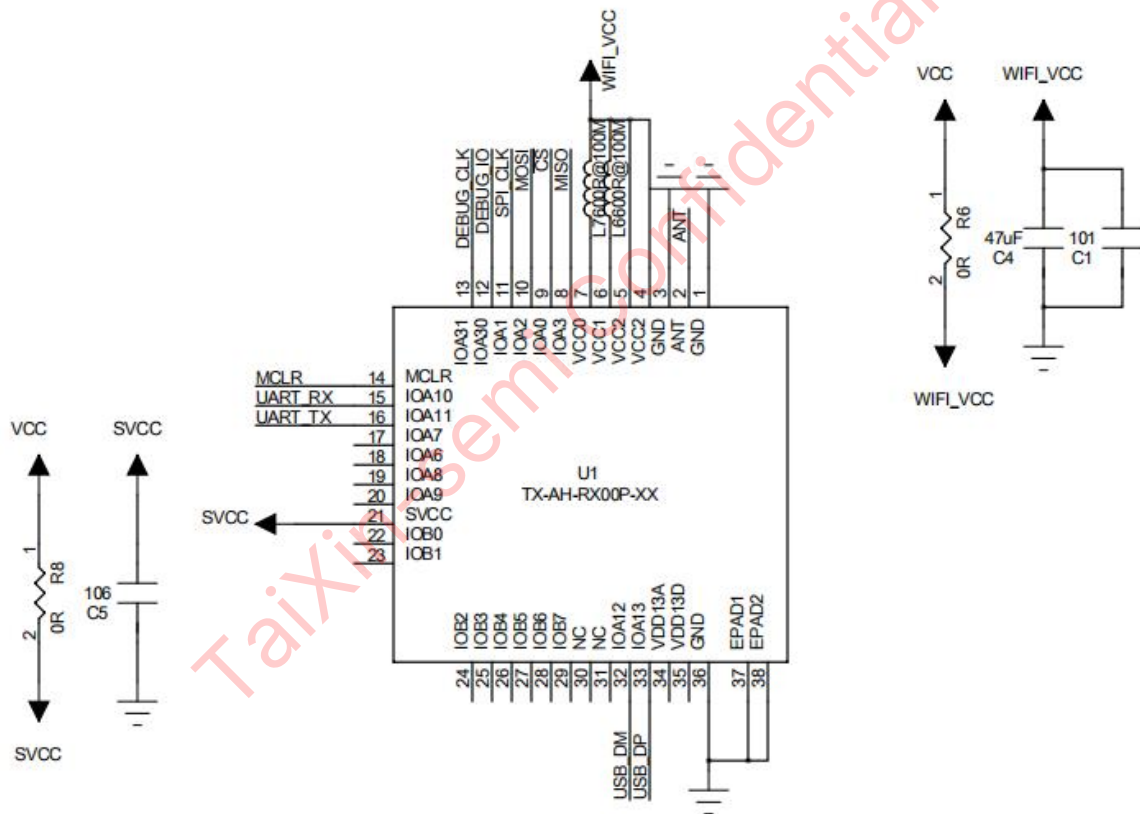


Figure 2-11 USB Interface Signal Connection

2.5.4. UART

When using the UART interface for transmission, UART0 is used as the data transmission interface, and UART1 is used as the debug print interface. SVCC needs to be powered and can be connected to the module's power supply, as shown in Figure 2-12.

Please note that to prevent leakage current in the serial port, a 1K resistor should be placed in series with TX/RX.

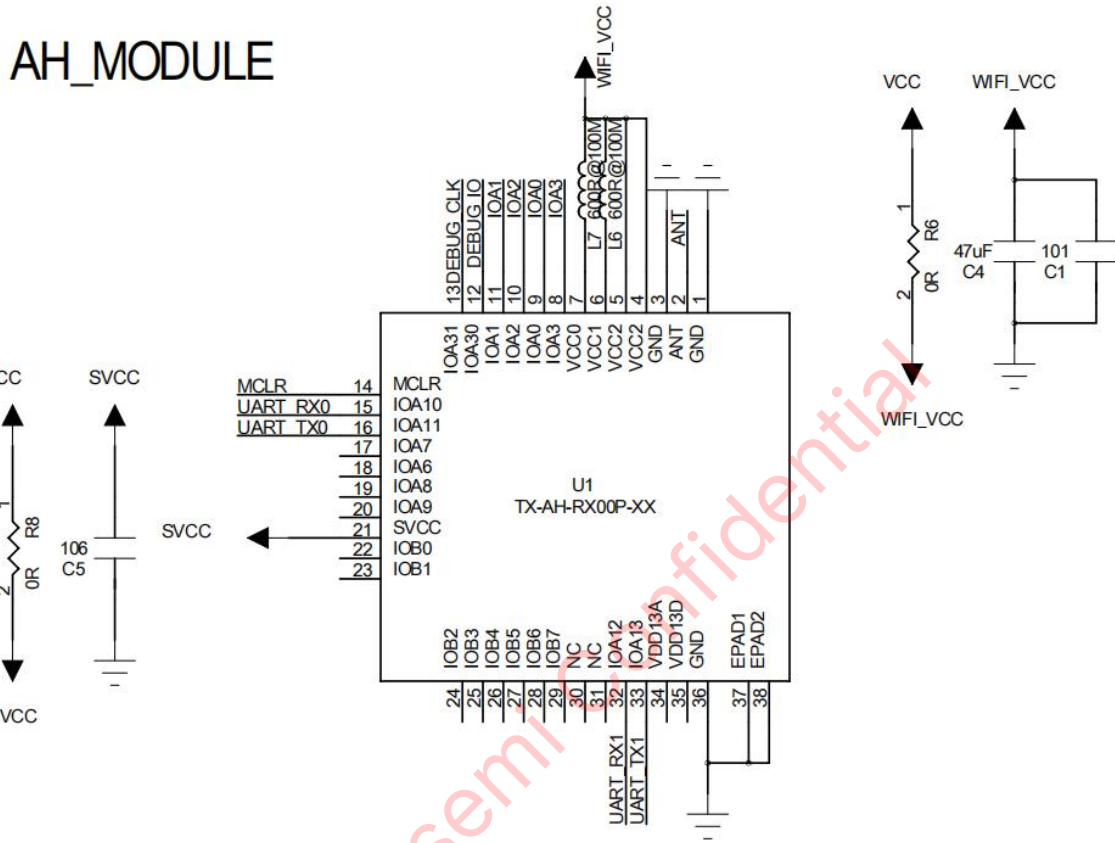


Figure 2-12 (a) UART Interface Signal

AH UART0

AH UART1



Figure 2-12 (b) UART Interface Signal

2.5.5. SPI

The TX-AH module supports up to two SPI interfaces, and the current function of SPI0 is mainly used for Boot. Please refer to Figure 2-5. If fast boot support is not needed, users can also use SDIO BOOT or USB BOOT methods.

If the system needs to use SPI as a communication interface, another set of SPI1 pins (PIN15~20) can be used for data communication and interaction with other systems. Note that it is recommended to power SVCC from the host controller.

IOA12/13 are used as debug print ports.

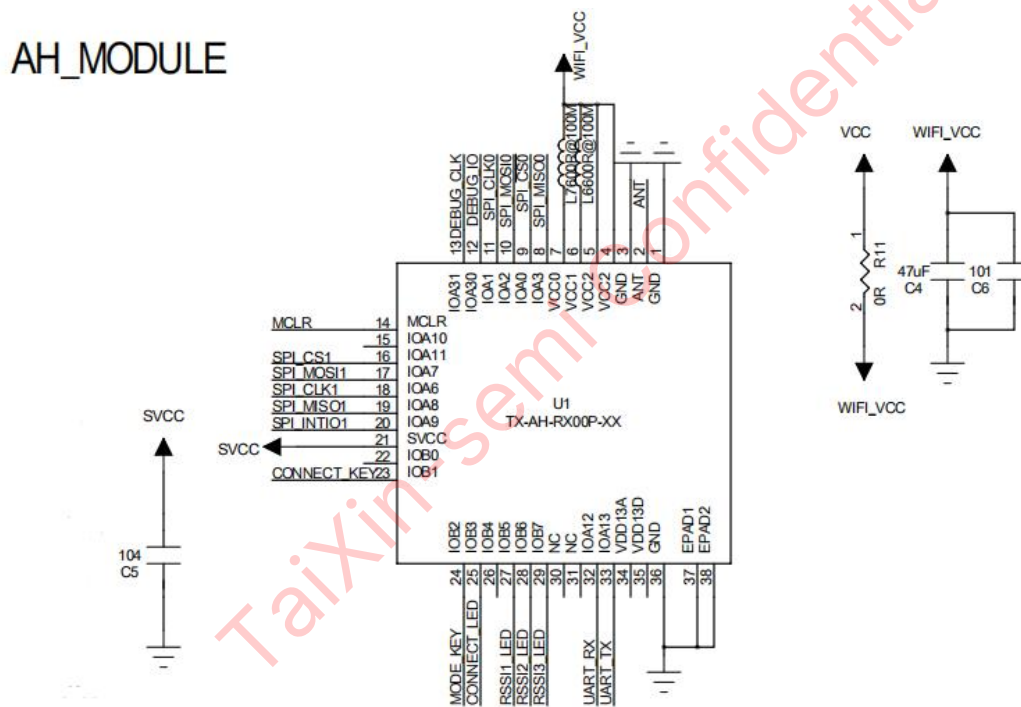


Figure 2-13 SPI Interface Signal

2.6. Low Power Consumption

2.6.1. STA Low Power Consumption

For STA low power, an external 1.3V DC-DC is required to supply power to the module's 1.3V power pins (PIN34/35), refer to section 2.1.3.

According to the method where PIN4/5/6/7 share one power supply, the STA's keep-alive current is approximately 240 μ A. For even lower keep-alive current, you can power PIN4/5/6 and PIN7 separately, cutting off power to PIN4/5/6 during sleep. This approach can save an additional 40 μ A of sleep power consumption (see the VCC1/VCC2 reference circuit in Figure 2-2). The separated power supply for STA's keep-alive current is approximately 200 μ A. Decide whether to power VCC1/VCC2 separately based on your design specifications.

The MCU wakes the AH module in the STA low power solution using the circuit in Figure 2-13. When the AH module enters deep sleep and needs to be woken by the MCU, MCLR should receive a negative pulse signal of approximately 500 μ s. A transistor is used to control the MCLR circuit to prevent undefined states in the host controller's IO output levels.

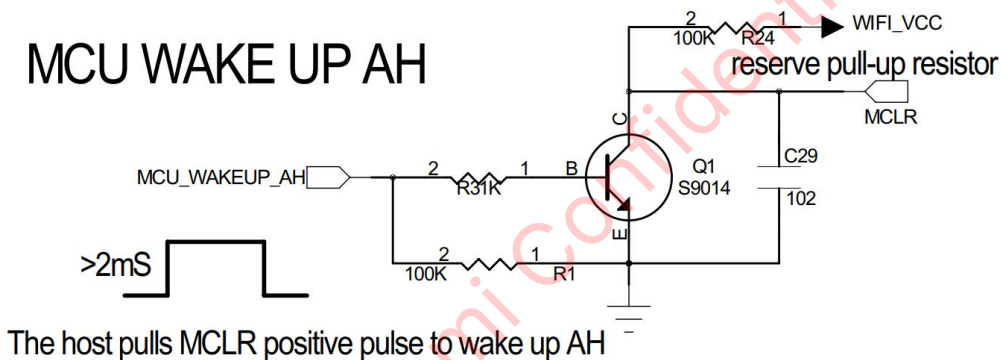


Figure 2-13 MCU Wake-Up AH Circuit

If the master control can not control the pulse of pulling 500 μ s wake-up time well, the pulling time may be longer which will cause the module to generate reset; then other IOs can be considered to use to do wake-up, and the driver interface can be configured through the master control to modify the wake-up IOs.

The AH module wakes the host controller in the STA low power solution using the circuit in Figure 2-14. Upon receiving a network packet wake-up command, the AH module quickly resumes normal operation. IOB0 outputs a 2ms pulse signal to the MCU, which then wakes up the host control system. Since the IOs in the IOB group are in an undefined state after entering deep sleep, a pull-down resistor is needed to ensure IOB0 is low during deep sleep. See Figure 2-12 for the reference schematic.

AH WAKE UP MCU

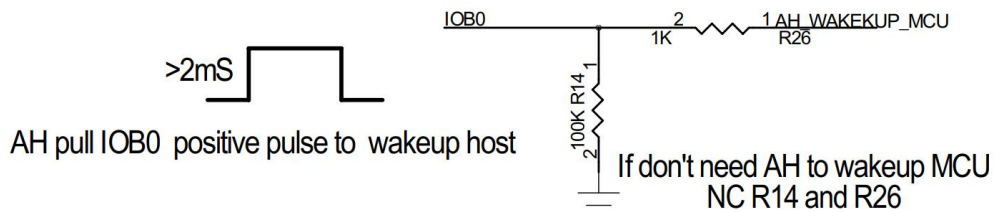


Figure 2-14 AH Wake-Up Host Controller Circuit

For fast booting in the STA low power solution, it is recommended to load the firmware using SPI nor-flash boot.

2.6.2. AP Low Power Consumption

Since the sleep current of AP low power consumption can be as low as the 5mA level (interfaces turned off) or 10mA level (interfaces not turned off). Therefore, for the AP low power consumption power supply circuit, connect PIN4/5/6/7 directly to a constant 3.3V supply, there is no need to separately power VCC1/VCC2. However, an external 1.3V DC-DC is required to supply power to the module's 1.3V power pins (PIN34/35), as referenced in section 2.1.3.

In the case of AP low power consumption at 5mA, interfaces are not kept active, and the MCU cannot wake the AH module through the interface. The wake-up circuit in Figure 2-13 is needed.

In the case of AP low power consumption at 10mA, interfaces remain active, allowing the MCU to wake the AH module through the interface, so the wake-up circuit in Figure 2-13 is not needed.

It is recommended to reserve IOB0 for the AH module to wake up the master control.

3. PCB Design

3.1. PCB Design Points

It is recommended to use a four-layer board design with the following layers:

- 1) Top layer: primarily for signal traces and component placement.
- 2) Second layer: ground layer with no signal traces to ensure a complete ground plane.
- 3) Third layer: power layer, where signal traces can be routed moderately while maintaining a complete ground plane beneath RF signals.
- 4) Bottom layer: should not have components placed on it; power traces should be routed on this layer.

3.2. Module Placement on the Baseboard

When placing the module on the baseboard, ensure that RF traces are kept as far away as possible from onboard DC-DC converters, other host controller oscillators, clocks (SDCLK, RMII_50M_CLK), and high-speed digital signal lines (such as HDMI, DDR, MIPI, etc.).

3.3. Power Supply

For power supply routing, a four-layer board design is recommended. Power traces should be routed on the fourth layer (bottom layer), with the main power trace width being at least 25 mil. Use at least two vias at layer transitions. To ensure RF performance, the power supply ripple peak-to-peak value must be <30 mV.

Before the power trace enters the module, at least one 10 μ F capacitor should be added, paired with a 0.1 μ F capacitor. After that, the power trace can branch off in a star configuration to reduce coupling between different power pins. All decoupling capacitors should be placed close to their respective power pins, with ground vias for the decoupling capacitors placed nearby to ensure a short return path.

Under the module, ensure at least nine ground vias connect to the ground plane. For the thermal pad (EPAD) under the chip on the module's backside, it is recommended to use a cross-hatch pattern with ink covering the gaps, as shown in Figure 3-1. Ground vias should be placed in these gaps to effectively reduce solder leakage when the module is soldered to

the baseboard.

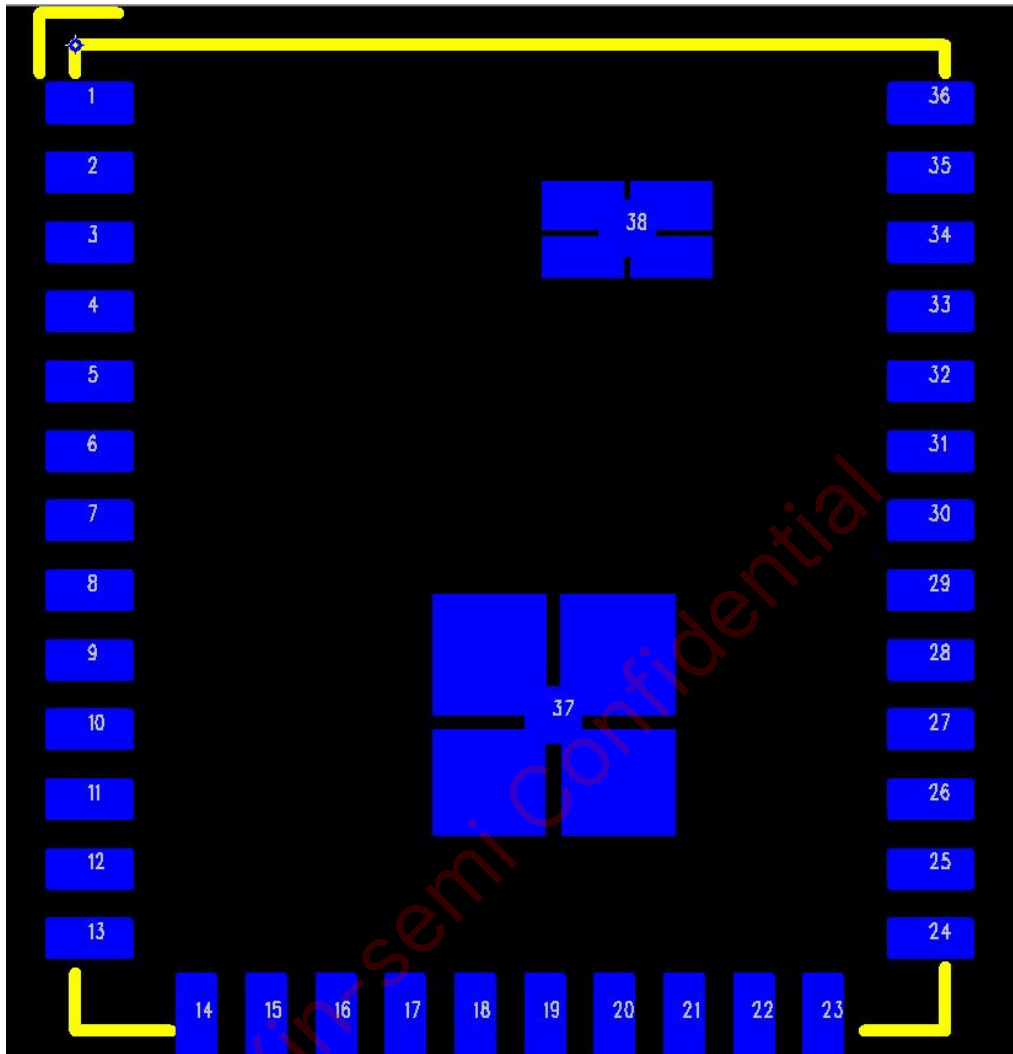


Figure 3-1 Module PCB Package

3.4. RF

RF traces must be designed with 50Ω single-ended impedance control, referencing the second layer as the ground plane. A PI-type matching circuit should be reserved on the RF trace and placed as close to the antenna end as possible.

The RF trace length should be as short as possible, with dense ground via shielding around it and a ground via spacing of 1-2mm.

RF trace width should be consistent, with no branching.

RF traces should stay on the top layer, and should not change layers or add vias, and should use 135° bends or curved traces. Ensure a complete ground plane on adjacent layers, with no other traces under the RF trace. Avoid placing high-frequency signal lines near RF traces. Antennas should be kept away from all high-frequency signal-transmitting components, such as oscillators, DDR, and other high-frequency clocks. Additionally, USB ports, USB to serial chips, Ethernet and UART signal lines (including traces, vias, test points, and pin headers) must be kept as far away from the antenna as possible. UART signal lines should be surrounded by ground vias for shielding.

For 50Ω single-ended impedance control, refer to the PCB stack-up design shown in Figure 3-2. SI9000 can be used for trace simulation calculations.

Thickness(mm)	Impedance(ohm)	Copper Distance(mil)	Trace Width(mil)	Copper Distance(mil)
-	50	12.2	12.6	12.2

Stack-up	Material	Base Copper Thickness(oz)	Thickness (mil)	Dielectric Constant
Solder Mask Layer			0.4	4
L1_Top	Finished Copper Thickness 1 oz		0.8	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core Board		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished Copper Thickness 1 oz		0.8	
Solder Mask Layer			0.4	4

Figure 3-2 PCB Parameters

Below are several examples of 50-ohm matching trace designs for different board layers based on SI9000 simulation. Since 50Ω matching depends on the PCB manufacturer's process, these are for reference only:

- 1) 0.6mm board thickness, 2 layers, 20.5mil trace width, 6mil ground spacing.

			Tolerance	Minimum	Maximum
Substrate 1 Height	H1	20.0000	0.0000	20.0000	20.0000
Substrate 1 Dielectric	Er1	4.0500	0.0000	4.0500	4.0500
Lower Trace Width	W1	20.5000	0.0000	20.5000	20.1000
Upper Trace Width	W2	20.0000	0.0000	20.0000	20.0000
Ground Strip Separation	D1	6.0000	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.7000	0.0000	1.7000	1.7000
Coating Above Trace	C2	0.5000	0.0000	0.5000	0.5000
Coating Dielectric	CEr	3.4000	0.0000	3.4000	3.4000
Impedance	Zo	49.51		49.51	49.51

2) 0.8mm board thickness, 2 layers, 22.5mil trace width, 6mil ground spacing.

			Tolerance	Minimum	Maximum
Substrate 1 Height	H1	27.6000	0.0000	27.6000	27.6000
Substrate 1 Dielectric	Er1	4.0500	0.0000	4.0500	4.0500
Lower Trace Width	W1	22.5000	0.0000	22.5000	22.5000
Upper Trace Width	W2	22.0000	0.0000	22.0000	22.0000
Ground Strip Separation	D1	6.0000	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.7000	0.0000	1.7000	1.7000
Coating Above Trace	C2	0.5000	0.0000	0.5000	0.5000
Coating Dielectric	CEr	3.4000	0.0000	3.4000	3.4000
Impedance	Zo	50.45		50.45	50.45

3) 1.0mm board thickness, 2 layers, 25mil trace width, 6mil ground spacing.

			Tolerance	Minimum	Maximum
Substrate 1 Height	H1	35.4000	0.0000	35.4000	35.4000
Substrate 1 Dielectric	Er1	4.0500	0.0000	4.0500	4.0500
Lower Trace Width	W1	25.0000	0.0000	25.0000	25.0000
Upper Trace Width	W2	24.5000	0.0000	24.5000	24.5000
Ground Strip Separation	D1	6.0000	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.7000	0.0000	1.7000	1.7000
Coating Above Trace	C2	0.5000	0.0000	0.5000	0.5000
Coating Dielectric	CEr	3.4000	0.0000	3.4000	3.4000
Impedance	Zo	50.21		50.21	50.21

- 4) 1.6mm board thickness, 4 layers, referencing the second layer, 12.5mil trace width, 12mil ground spacing.

			Tolerance	Minimum	Maximum
Substrate 1 Height	H1	7.4100	0.0000	7.4100	7.4100
Substrate 1 Dielectric	Er1	4.0500	0.0000	4.0500	4.0500
Lower Trace Width	W1	12.5000	0.0000	12.5000	12.5000
Upper Trace Width	W2	12.0000	0.0000	12.0000	12.0000
Ground Strip Separation	D1	12.0000	0.0000	12.0000	12.0000
Trace Thickness	T1	1.4000	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.7000	0.0000	1.7000	1.7000
Coating Above Trace	C2	0.5000	0.0000	0.5000	0.5000
Coating Dielectric	CEr	3.4000	0.0000	3.4000	3.4000
Impedance	Zo	49.5		49.5	49.5

3.5. Interfaces

3.5.1. USB

The series resistors on the USB lines should be placed as close to the module as possible. Reserve space for TVS protection diodes, placing them near the exposed interface. USB_DM and USB_DP traces should be as short as possible and routed as differential pairs with a controlled differential impedance of 90Ω. Ensure the entire path is surrounded by ground traces and shielded with ground vias. If a ribbon cable connection is required, pay attention to USB line shielding, and it is strongly recommended to use a shielded ribbon cable.

3.5.2. SDIO

The series 22Ω resistors on the SDIO lines should be placed as close to the host controller as possible. SDIO traces should be kept as short as possible, and the SD_CLK trace should be surrounded by ground traces and shielded with ground vias along the entire path.

3.5.3. RMII

RMII traces should be kept as short as possible. Reserve an RC filter circuit for the 50MHz clock line and place it close to the Ethernet PHY. The Ethernet clock crystal oscillator should be placed as far from the module's RF traces as possible to avoid high harmonic interference

from the clock signal or high-speed digital signals affecting the module's RF performance.

3.5.4. UART

The series 1K Ω resistors on the UART lines should be placed as close to the module as possible. UART_TX and UART_RX traces should be kept as short as possible, with the entire path surrounded by ground traces and shielded with ground vias.

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4. PCB-Level EMI Measurement Method

Due to high-speed signals, power ripple, and other phenomena at the PCB level, they can easily be picked up by the antenna, impacting RF performance. When debugging circuit performance, it is necessary to assess whether the magnitude of EMI is significant enough to affect the operation of the RF.

By using the command "at+acs_start=1", you can observe the background noise (bg or BGR) across all channels. It is recommended to switch to a 2M bss_bw for assessment, which can be set using the command "at+bss_bw=2". Use the command "at+chan_list=?" to query the current operating frequency band with "at+chan_list=?" and set a series of 2MHz-spaced channels to cover the required operating band. For example, if "at+chan_list=9080, 9160, 9240" and bss_bw=8MHz, indicating an operational bandwidth of 904-928MHz, 2MHz-spaced channels should be set to: "at+chan_list=9030, 9050, 9070, ..., 9270". After configuring bss_bw and chan_list, input "at+acs_start=1" to receive the following results:

```
[100330] acs...
[100331] freq    pri_chn  bg_min  bg_avg  bg_max  rxsync_cnt => noise factor
[100363] 903000    0       -110    -107    -105    0         => -133
[100393] 903000    1       -111    -107    -100    0         => -132
[100423] 905000    0       -109    -104    -101    0         => -129
[100453] 905000    1       -112    -105    -102    0         => -130
[100483] 907000    0       -110    -104    -96     0         => -128
[100513] 907000    1       -111    -104    -96     0         => -128
[100543] 909000    0       -113    -108    -104    0         => -134
[100573] 909000    1       -113    -108    -104    0         => -134
[100603] 911000    0       -115    -109    -106    0         => -135
[100633] 911000    1       -115    -108    -60     0         => -123
[100663] 913000    0       -115    -112    -110    0         => -139
[100693] 913000    1       -115    -112    -111    0         => -139
[100723] 915000    0       -115    -109    -60     0         => -124
[100753] 915000    1       -116    -111    -106    0         => -137
[100783] 917000    0       -112    -109    -106    0         => -135
[100813] 917000    1       -114    -109    -101    0         => -134
[100843] 919000    0       -110    -106    -102    0         => -131
[100873] 919000    1       -109    -106    -102    0         => -131
[100902] 921000    0       -110    -97     -60     0         => -112
[100932] 921000    1       -109    -94     -60     0         => -109
[100938] acs result: freq=913000, prichn=0 nr=-278
[100943] notify freq: 913000
[100945] acs done
[103029]
```

Figure 4-1 acs_start Results

If the bg_avg of a channel is <-96dB, it indicates that EMI does not significantly interfere with the RF. If bg_avg is between -96dB and -90dB, the performance is suboptimal but still marginally acceptable, and improvements are advisable. If bg_avg is >-90dB, EMI significantly interferes with the RF, and rectification is recommended.

When measuring, ensure that the BGR degradation is not caused by external interference

rather than the board-level EMI. Testing in a shielded box is ideal; if unavailable, use a relatively enclosed room. During testing, the antenna should be placed as close as possible to its actual placement in the actual antenna layout of the solution.

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5. Methods for Improving RF Interference with Audio

5.1. Layout Recommendations

The audio circuit is susceptible to interference; therefore, it should be laid out at a distance from the RF section during design. As shown in the figure below.

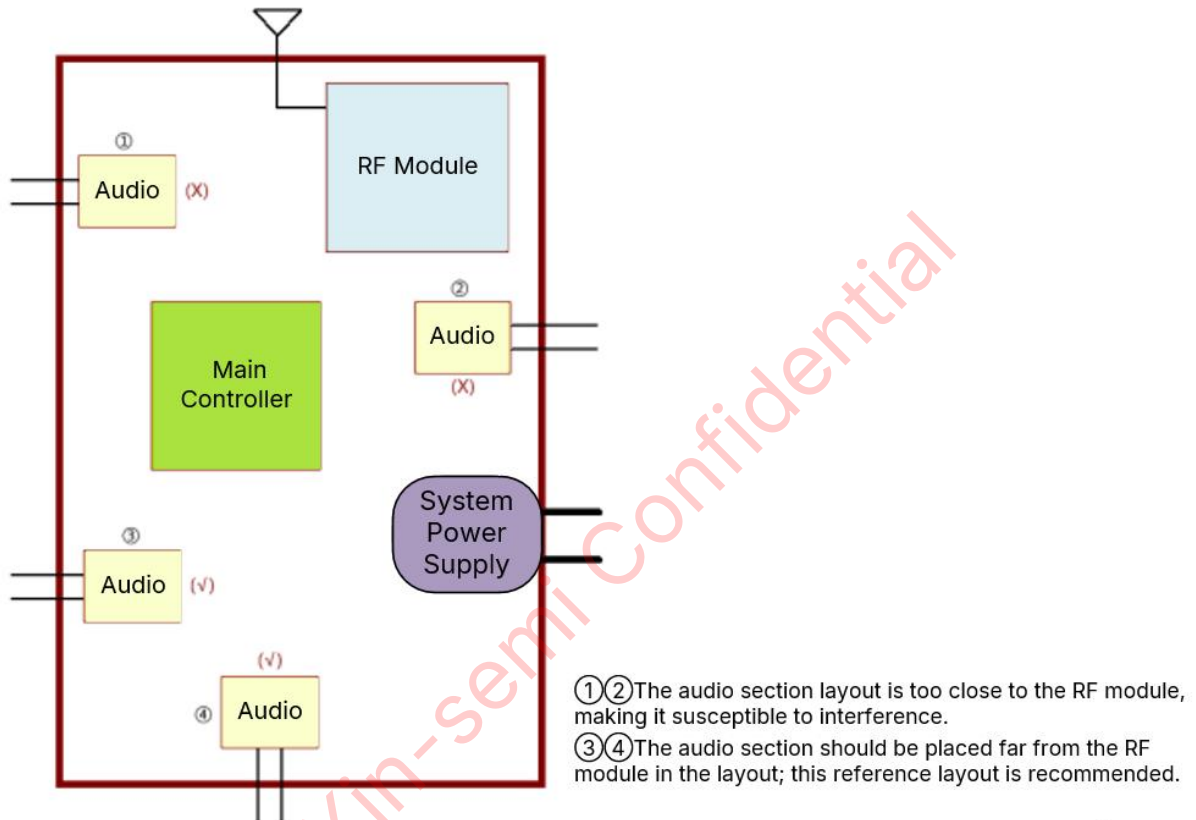


Figure 5-1 Reference Layout for Audio and RF Components

5.2. Circuit Optimization References

A typical and commonly used PA circuit usually performs adequately under normal circumstances.

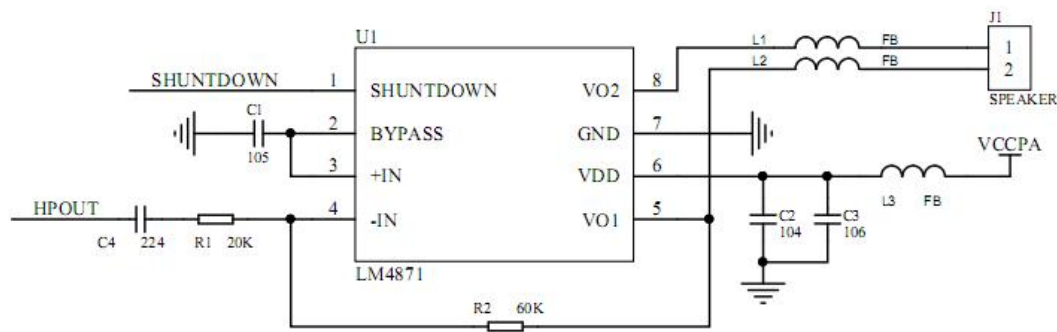


Figure 5-2 Conventional PA Circuit.

When encountering AH's TX (transmit), the PA (Power Amplifier) may be interfered with by the TX, resulting in a ticking noise at the frequency of the TX's switching frequency. The following points can be considered for rectification:

- 1) **Power Supply Section:** During AH TX, power supply fluctuations may occur. Therefore, the schematic provides two power supply paths, L3/L4, are reserved for PAVDD, allowing for selection between VCC33 or VBAT. A ferrite bead or a small resistor (1-2Ω) can be added in series for RC filtering. There are four possible combinations, and the best one should be chosen. Although an independent LDO power supply could be used, it is generally not preferred due to cost considerations.
- 2) **PA Output Circuit:** Reserve the filtering capacitors C5/C6 connected to ground to reduce interference from airborne radiation absorbed by the speaker wires. Twisting the wires can also help in reducing interference.
- 3) **PA Input Circuit:** Reserve a band-pass filter circuit, as shown below. The combination of R3/C8 (low-pass) and C7/R4 (high-pass) forms a band-pass filter. In the small signal model, C4/R1 also acts as a high-pass filter, which can attenuate some interference noise.
- 4) **Ground Loop Handling in PA Circuit:** The ground for the PA circuit and the filtering circuit should be connected to the main power supply through a dedicated ferrite bead L5, separating it from AH's digital ground. In battery-powered systems, considering the antenna's radiation mechanism and treating the antenna as an ideal dipole, the PCB ground plane acts as the reference plane for the dipole. Consequently, the entire ground plane experiences fluctuations. Using a ferrite bead to connect the analog ground to the power ground can reduce interference caused by ground plane fluctuations.

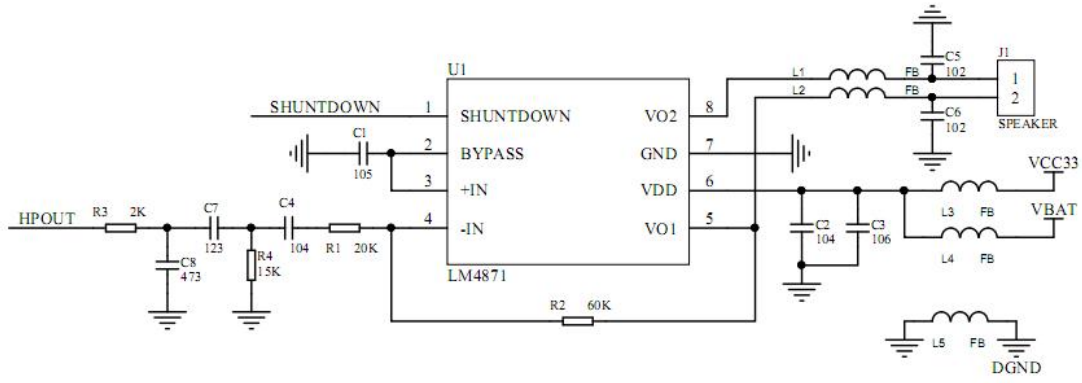


Figure 5-3: Optimized PA Circuit

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